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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/713,564	11/13/2003	Kuljit S. Bains	5038-301	8265

7590 11/05/2004

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EXAMINER	
IQBAL, NADEEM	

ART UNIT	PAPER NUMBER
2114	

DATE MAILED: 11/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/713,564	BAINS ET AL.	
	Examiner	Art Unit	
	Nadeem Iqbal	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *19-22* is/are allowed.

6)☒ Claim(s) *1-3,12 and 23* is/are rejected.

7)☒ Claim(s) *4-11,13-18 and 24-27* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103© and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

1. Claims 1-3, 12, & 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lawrence et al., (U.S. Patent number 5995424) in view of Hamamatsu et al., (U.S. Patent Application number 2003/0035328).

As per claim 1, Lawrence et al., teaches (col. 7, lines 3-5) a portable synchronous memory module tester for testing the function status of synchronous memories. He also teaches (col. 7, lines 12-14) an SDRAM module is placed into one of UUT sockets and a user interface program is executed (See Fig. 1, Fig. 2). He thus teaches the coupling a tester to a DIMM and coupling a plurality of DRAM modules that are located on the DIMM and testing the plurality of DRAM modules. He does not explicitly disclose coupling a tester to a buffer chip that is located on a DIMM using a first set of pins on the buffer chip. Hamamatsu et al., teaches (Page 2, col. 1,

lines 4-6) a peripheral circuit for inputting and outputting data to and from the plurality of memory cells, and a test mode circuit. He also teaches (page 2, col. 1, lines 28-31) a semiconductor memory device provided with a buffer circuit, which converts the externally supplied signal to the signal formed of the voltage level used in the module. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to include the invention of Hamamatsu into the invention of Lawrence to be able to couple the tester of Lawrence to buffer located on the SDRAM module using a first set of pins and to a second set of pins on the buffer. This is because Lawrence already teaches testing the SDRAM module having buffers and Hamamatsu teaches a peripheral circuit for inputting and outputting data to and from the plurality of memory cells, and a test mode circuit, thus provides motivation for the stated inclusion.

As per claims 2 & 3, Hamamatsu et al., teaches (Page 2, col. 1, lines 11-13) testing a special operation of each of the plurality of memory cells in response to the test mode signal, therefore would also couple tester to a first set of pins during a non-test operation mode. He also teaches that (col. 2, lines 42-44) that for shifting to the test mode, the two power supply voltages with different voltage levels are supplied to the memory device.

As per claims 12 & 23, Lawrence et al., substantially teaches the claimed invention as disclosed related to claim 1 above. He also teaches (col. 7, lines 12-14) an SDRAM module is placed into one of UUT sockets and a user interface program is executed (See Fig. 1, Fig. 2). He thus teaches the coupling a tester to a DIMM and coupling a plurality of DRAM modules that are located on the DIMM and testing the plurality of DRAM modules. He does not explicitly disclose coupling a tester to a buffer chip that is located on a DIMM using a first set of pins on

the buffer chip. Hamamatsu et al., teaches (Page 2, col. 1, lines 4-6) a peripheral circuit for inputting and outputting data to and from the plurality of memory cells, and a test mode circuit. He also teaches (page 2, col. 1, lines 28-31) a semiconductor memory device provided with a buffer circuit, which converts the externally supplied signal to the signal formed of the voltage level used in the module. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to include the invention of Hamamatsu into the invention of Lawrence to be able to couple the tester of Lawrence to buffer located on the SDRAM module using a first set of pins and to a second set of pins on the buffer. This is because Lawrence already teaches testing the SDRAM module having buffers and Hamamatsu teaches a peripheral circuit for inputting and outputting data to and from the plurality of memory cells, and a test mode circuit, thus provides motivation for the stated inclusion.

Allowable Subject Matter

2. Claims 19-22 are allowed.

3. Claims 4-11, 13-18, 24-27 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nadeem Iqbal whose telephone number is (703)-308-5228. The examiner can normally be reached on M-F (8:00-5:30) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W Beausoliel can be reached on (703)-305-9713. The fax phone numbers for the organization where this application or proceeding is assigned are (703)-746-7239 for regular communications and (703)-746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)-305-3900.

Nadeem Iqbal
Primary Examiner
Art Unit 2184